MULTICHIP IMPATT POWER COMBINING, A SUMMARY WITH NEW RESULTS

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Abstract

X-band IMPATT diode chips have been efficiently combined in parallel, in series on diamond, stacked with diamond heat sinks and using lumped element circuit techniques with mode suppression. Combined device types include c.w. silicon p^+-n-n^+, c.w. GaAs Schottky lo-hi-lo, pulsed GaAs p^+-hi-lo and pulsed GaAs double-drift. This paper will summarize tasks performed over a four year period and will attempt to place some of the results in perspective with respect to practical applications. Work at 35 GHz, begun in December 1978, will also be described.

Introduction

Experiments with various IMPATT diode chips have provided data which show that IMPATT chips can be efficiently combined in a variety of multichip configurations if certain instabilities are eliminated. X-band assemblies have been configured in series-on-diamond, in parallel, in series-parallel-on-diamond and using lumped circuit elements. Several device types (Table 1) have been combined efficiently (90% or higher) and stably (no spurious modes) in one or more of the configurations but not all combine readily with the same approach or with equal ease. With GaAs device chips, the inherent chip parameter variations within a batch do not constitute an inordinate problem but modification of the multichip configurations is required in some instances to accomodate batch-to-batch variations. The more efficient devices are oftentimes somewhat difficult to combine. Silicon c.w. p^+-n-n^+ chips (efficiency ≈ 5-8%) are an exception to this observation and combine in series only with great difficulty.

TYPE OF CHIP	SOURCE
C.W. silicon p^+-n-n^+	Georgia Tech
C.W. GaAs Schottky lo-hi-lo	Raytheon
Pulsed GaAs p^+-hi-lo	Varian
Pulsed GaAs double-drift	Raytheon

Table 1. Types of IMPATT Chips and Suppliers

Multichip Geometries

Multiple mesa IMPATT chips, wherein all the mesas are connected in parallel in a microwave package, have been used by many diode manufacturers and are not discussed herein. Some interesting experiments with this type of device were reported earlier, however, in Transactions MTT-S[1]. A multichip IMPATT consists of two or more separate IMPATT chips connected in some compact way to achieve stable oscillation or amplification with higher power output and high combining efficiency. Primary emphasis has been with chips connected electrically in series on diamond. Figure 1 shows several possible geometries for such devices. Early experiments were performed using two IMPATT chips on a single diamond heat sink mounted in a conventional diode package as shown in the upper sketch (A). Other experiments used the unpackaged configuration of sketch (B). Neither of these arrangements provided stable addition of the respective chip powers except at very low current density. To correct this problem, quartz capacitors were placed in parallel with each diode chip as shown by sketches (C) and (D). Both (C) and (D) allowed stable maximum power operation.

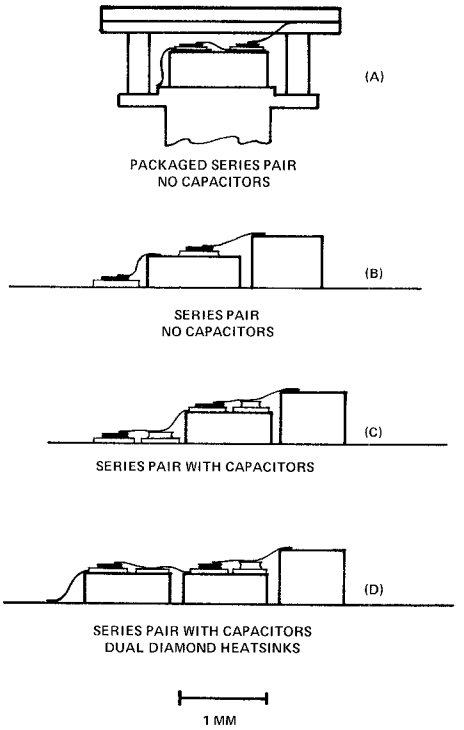


Figure 1. Possible Multichip Geometries

Figure 2 shows a typical geometry constructed on a half inch diameter copper slug for handling and mounting in a water cooled r.f. test fixture. All the devices have been constructed on copper slugs and tested in the r.f. fixture of Figure 3.

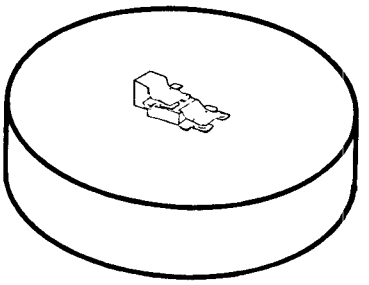


Figure 2. Multichip Assembly on Copper Slug

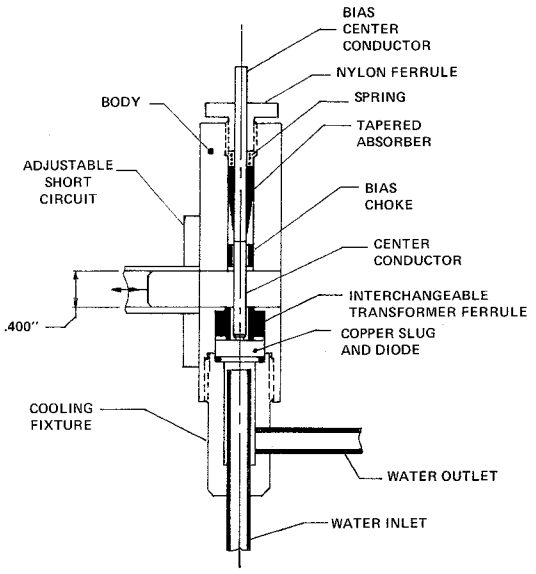


Figure 3. R.F. Test Fixture

R.F. Performance

The most significant X-band results achieved thus far were with c.w. GaAs Schottky lo-hi-lo and pulsed GaAs p^+-hi-lo chips. These results are summarized in figures 4 and 5. Each figure shows detailed SEMS of typical assemblies. The accompanying tables include data measured on several similar assemblies. The overall size of each assembly can be estimated by noting that each of the diamond heat sinks is ≈ .040" square. Only a small number of pulsed double drift chips was available for tests but good results were also obtained with these chips. Table 2 summarizes performance obtained with the individual devices and with two devices connected in series.

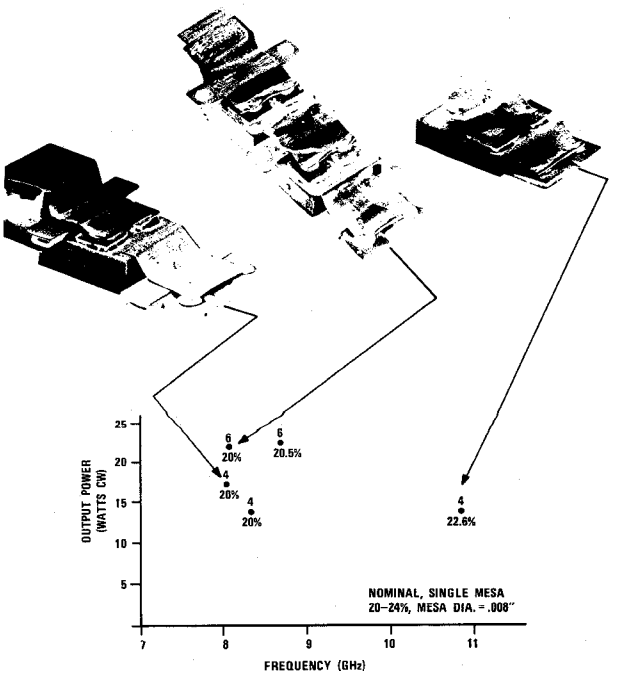
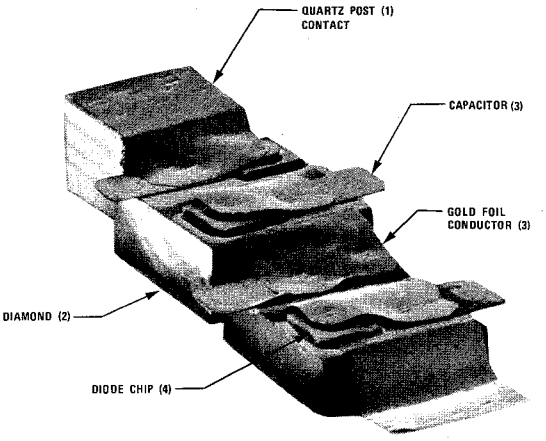


Figure 4. R.F. Results (C.W.)



No. Chips	(V) V_p	(A) I_p	(W) P_p	(W) P_o	(%) η	(GHz) f_o	(μsec) P.W.	(%) Duty
1(typical)	40/50	1.3/1.6	-	10/14	15/18	10/12	1	20
2(series)	90	1.40	126.0	21.2	16.8	11.0	1	20
3(series)	140	1.35	189.0	32.2	17.0	11.0	1	20
	150	1.43	214.5	35.1	16.4	11.0	1	20
4(series)	170	1.43	243.1	60.4	24.9	11.5	1	20

Figure 5. R.F. Results (Pulsed)

DUTY = 20% PULSE WIDTH = 1 MICROSECOND

PARAMETER	SINGLE CHIP	SERIES PAIR
Po(Peak)	15-17 W	28.5 W
Efficiency	16-19 %	16-17 %
Frequency	11.5-12.5 GHz	12.2 GHz

Table 2. Performance with Pulsed Double-drift Diode Chips

Multichip Assembly

All multichip assemblies were fabricated using relatively standard semiconductor laboratory tooling and equipment. Figure 6 is a sketch of the four chip 60W pulsed diode of Figure 5. The device is typical and was prepared and assembled in the following manner.

1) The 1 mm square x .5 mm thick diamond heat sinks were cleaned and metallized, top and bottom, with 0.07 microns of evaporated chromium followed by 0.2 microns of evaporated gold. The gold was followed by an additional 4 microns of electroplated gold.

2) The diamonds were next mounted on a glass slide and masked using black wax to obtain the desired separate metallized pads evident on the top surface of each diamond. This step also removed residual metallization unavoidably deposited on the sides of the diamond heat sinks.

3) The diamond heat sinks were then compression bonded to a gold plated, annealed copper slug using a diamond tipped bonding stylus. Pressure of 25 KPSI and temperature of 300°C were used. In some instances, a somewhat higher pressure was used to press the diamond part way into the copper slug. The lower right hand heat sink of Figure 6 has been treated in this manner.

4) Next, the stabilization capacitors were compression bonded at 300°C and 15 KPSI and the quartz contact post was soldered or t.c. bonded in place.

5) Prior to final assembly, the diode chips were soldered in place using an induction heated collar and 80/20 Au Sn solder at 280°C. Since each diode required a separate solder cycle, the cycle length (time at solder temperature) was minimized so as to prevent damage to previously soldered chips. The cycle was terminated by injection of hydrogen as a rapid-cool gas.

6) As a final step, gold foil was cut to the desired dimensions and t.c. bonded at 275°C utilizing a sapphire bonding wedge.

The foregoing process is tedious and requires considerable skill. Given the large number of devices and multichip geometries fabricated, it was not practical to use jigs, fixtures, and photolithography to simplify metallization and assembly. The diode chips were used as-received from the vendors. The chips were of the plated heat sink type and required solder bonding. Therefore, other mounting means, such as thermocompression bonding, could not be used to mount the chips. Finally, the interconnections, chip-to-chip, could be simplified by use of a beam-leaded approach. Diodes having beam leads were unavailable.

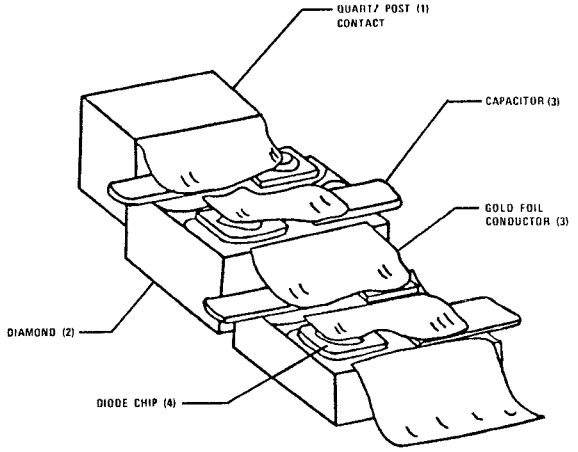


Figure 6. Sketch, Four Chip, 60 Watt Pulsed Diode Assembly

Problems

The most severe problems encountered were with instabilities and power saturation in series-connected silicon p^+-n-n^+ chips. These problems, which were observed only with series connected chips, were controlled by attaching quartz capacitors in parallel with the individual chips as previously noted. Gallium Arsenide multichip assemblies did not exhibit the same problems but bias circuit oscillations and related failures were considerably reduced and often eliminated entirely by use of the capacitors.

In order to ensure that infant failures of individual chips would not destroy all the chips in the multichip assemblies, all chips were placed under mechanical pressure on a heat sink and prestressed electrically. Failed chips were discarded. The chips were then matched according to breakdown and according to the slopes of the respective breakdown curves during the prestress test. In general, chips mounted in parallel were matched for breakdown and slopes within a volt or two. Series chips were matched within much broader limits of 3 to 6 volts.

Late Results - 35 GHz

Work at 35 GHz was started in December 1978. Progress toward realization of 35 GHz c.w. and pulsed multichip assemblies will be reported. Initial scaling and calculations indicate that the X-band approaches should extend to 35 GHz with reasonable effort. Extension of series-connected multichips to even higher frequencies is thought possible but will require modifications to both the device chip geometry and chip mounting geometries.

Acknowledgements

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